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PTO/SB/21 (modified)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM <i>(to be used for all correspondence during pendency of filed application)</i>	U.S. Department of Commerce Patent and Trademark Office	Application Number	10/020,558
		Filing Date	December 14, 2001
		First Named Inventor	Sol P. DiJaili
		Group Art Unit Number	2811
		Examiner Name	Not yet known
Total Number of Pages in This Submission 9*		Attorney Docket Number	21153-05927

ENCLOSURES (check all that apply)	
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REMARKS: *Number of pages does not include cited references

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Signature:		
Attorney/Reg. No.:	Michael Plimier, Reg. No.: 43,004	Dated: May 1, 2002

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I hereby certify that this correspondence, including the enclosures identified above, is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231 on the date shown below. If the Express Mail Mailing Number is filled in below, then this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service pursuant to 37 CFR 1.10.		
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21153/05927/DOCS/1263428.1

PTO/SB/17 (10-01)(modified)
OMB 0651-0032

Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

0002/PTO(modified)
Rev. 10/2001U.S. Department of Commerce
Patent and Trademark Office**FEE TRANSMITTAL****TOTAL AMOUNT OF PAYMENT**

Subtotal (1) + Subtotal (2) + Subtotal (3) =

(\$)**0.00****Complete if Known**

Application Number	10/020,558
Filing Date	December 14, 2001
First Named Inventor	Sol P. DiJaili
Group Art Unit	2811
Examiner Name	Not yet known
Attorney Docket Number	21153-05927

METHOD OF PAYMENT**1. The Commissioner is hereby authorized to:**

- ☐ Charge the indicated fees to the below mentioned deposit account.
- ☒ Charge any additional fee required under 37 CFR 1.16 - 1.21 or credit any over payments to the below mentioned deposit account. †
- ☐ Applicant claims small entity status See 37 CFR 1.27

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2. ☐ Payment Enclosed:☐ Check ☐ Credit Card ☐ Other**FEE CALCULATION (fees effective 10/01/2001)****1. FILING FEE**

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due
101/\$740	201/\$370	Utility Filing	<input type="text"/>
106/\$330	206/\$165	Design Filing	<input type="text"/>
108/\$740	208/\$370	Reissue	<input type="text"/>
114/\$160	214/\$80	Provisional Filing	<input type="text"/>
SUBTOTAL (1)			(\$)0.00

2. CLAIMS

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description
103/\$18	203/\$9	Claims in excess of 20
102/\$84	202/\$42	Independent claims in excess of 3
104/\$280	204/\$140	Multiple dependent claim
109/\$84	209/\$42	Reissue independent claims over original patent
110/\$18	210/\$9	Reissue claims in excess of 20 and over original patent

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Fee Code/Fee	Small Entity Fee Code/Fee	Fee Description	Fee Due
105/\$130	205/\$65	Surcharge - late filing fee or oath	<input type="text"/>
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119/\$320	219/\$160	Notice of Appeal	<input type="text"/>
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142/\$1,280	242/\$640	Utility Issue Fee (Or Reissue)	<input type="text"/>
143/\$460	243/\$230	Design Issue Fee	<input type="text"/>
122/\$130	122/\$130	Petitions to the Commissioner	<input type="text"/>
126/\$180	126/\$180	Submission of Information Disclosure Statement	<input type="text"/>
179/\$740	279/\$370	Request for Continued Examination (RCE)	<input type="text"/>
581/\$40	581/\$40	Recording each patent assignment per property (times number of properties)	<input type="text"/>
146/\$740	246/\$370	Filing a submission after final rejection (37 CFR 1.129(a))	<input type="text"/>
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[] First presentation of multiple dependent claim							

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SUBTOTAL (2) (\$)**0.00****SUBMITTED BY**Typed or Printed Name **Michael Plimier**

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Complete (if applicable)Reg. Number **43,004**

Date

May 1, 2002

21153/05927/DOCS/1263429.1



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Sol P. DiJaili, Jeffrey D. Walker and John M. Wachsman
APPLICATION NO.: 10/020,558
FILING DATE: December 14, 2001
TITLE: Optical Logical Circuits Based on Lasing Semiconductor Optical Amplifiers
EXAMINER: Not yet known
GROUP ART UNIT: 2811
ATTY. DKT. NO.: 21153-05927

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P-3
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WASHINGTON, DC. 20231

INFORMATION DISCLOSURE STATEMENT

Under 37 CFR §§ 1.56 and 1.97-98

SIR:

Pursuant to the provisions of 37 CFR §§ 1.56 and 1.97-98, enclosed herewith is modified form PTO-1449 listing references for consideration by the Examiner. Enclosed is a copy of each listed references that may be material to the examination of this application, and for which there may be a duty to disclose.

The filing of this Information Disclosure Statement shall not be construed as a representation regarding the completeness of the list of references, or that inclusion of a reference in this list is an admission that it is prior art or is pertinent to this application, or that a search has been made, or as an admission that the information listed is, or may be considered to be, material to patentability, or that no other material information exists, and shall not be construed as an admission against interest in any manner.

This Information Disclosure Statement is being filed:

- ☒ within three months of the filing date of the application, or date of entry into the national stage of an international application, or before the mailing date of a first office action on the merits, whichever event last occurred;

- ☐ before the mailing of a first official action after the filing of a request for continued examination (RCE) under 37 CFR § 1.114;
- ☐ after three months of the filing date of this national application or the date of entry of the national stage in an international application, or after the mailing date of the first official action on the merits, whichever event last occurred, but before the mailing date of the first to occur of either: (1) a final action under 37 CFR § 1.113; or (2) an action that otherwise closes prosecution in the application, and:
 - ☐ attached hereto is the fee set forth under 37 CFR § 1.17(p) for submission of this Information Disclosure Statement under 37 CFR § 1.97(c); OR
 - ☐ Applicant certifies pursuant to 37 CFR § 1.97(e) that:
 - ☐ each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; OR
 - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement;
- ☐ before the payment of the issue fee but after the mailing date of the first to occur of either: (1) a final action under 37 CFR § 1.113; or (2) an action that otherwise closes prosecution in the application, and:
 - ☐ Applicant certifies pursuant to 37 CFR § 1.97(e) that:
 - ☐ each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; or
 - ☐ no item of information contained in this Information Disclosure Statement was cited in a communication from a

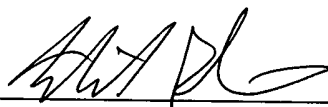
foreign patent office in a counterpart foreign application and, to the knowledge of the person signing this certification after making reasonable inquiry, no item of information contained in this Statement was known to any individual designated under 37 CFR § 1.56(c) more than three months prior to the filing of this Statement; AND

- ☐ attached hereto is the fee set forth under 37 CFR §1.17(p) for submission of this Information Disclosure Statement under 37 CFR. § 1.97(c); OR
- ☐ after the payment of the issue fee. Applicant request that the information contained in this Information Disclosure Statement be placed in the file according to 37 CFR § 1.97(i), although the information may not be considered by the USPTO.
- ☐ This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior application No. _____, filed on _____, and the references cited therein are hereby referenced, but are not required to be provided in this application under 37 CFR § 1.98(d).
- ☐ Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not received by any individual designated in 37 CFR § 1.56(c) more than thirty days prior to the filing of this Information Disclosure Statement. 37 CFR § 1.704(d).
- ☒ Applicant submits that no fee is required for the consideration of this Information Disclosure Statement.

Consideration of the listed references and favorable action are solicited.

Respectfully submitted,
Sol P. DiJaili, Jeffrey D. Walker
and John M. Wachsman

Dated: May 1, 2002

By: 
Michael Plimier, Reg. No.: 43,004
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Sheet 1 of 3

FORM PTO-1449
(REV. 6-89)U.S. DEPARTMENT OF COMMERCE
Patent and Trademark OfficeAttorney's Docket No.
21153-05927Serial No.
10/020,558**INFORMATION DISCLOSURE CITATION**

(Use several sheets if necessary)

Applicants

Sol P. DiJaili et al.

Filing Date
December 14, 2001Group Art Unit
2811**U.S. PATENT DOCUMENTS**

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	A	6,335,992	01-01-02	Bala et al.	385	17	02-15-00
	B	6,333,799	12-25-01	Bala et al.	359	128	01-06-98
	C	6,317,531	11-13-01	Chen et al.	385	17	
	D	6,128,115	10-03-00	Shiragaki	359	128	
	E	6,115,517	09-05-00	Shiragaki et al.	385	24	
	F	6,061,156	05-09-00	Takeshita et al.	359	117	
	G	5,999,293	12-07-99	Manning	359	139	
	H	5,771,320	06-23-98	Stone	385	16	
	I	5,436,759	07-27-95	Dijaili et al.	359	333	
	J	5,305,412	04-19-94	Paoli	385	122	
	K	5,299,054	03-29-94	Geiger	359	251	
	L	4,794,346	12-27-88	Miller	330	4.3	
	M	3,828,231	08-06-74	Yamamoto	357	30	
	N	3,467,906	09-16-69	Cornely et al.	330	4.3	

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	O	56006492	01-23-81	Japan	H01S	3/18		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	P	Alcatel, "Alcatel Optronics Introduces a Gain-Clamped Semiconductor Optical Amplifier," <i>Press Release for Immediate Publication</i> , OFC '98, San Jose, 1 unnumbered page, (Feb. 1998).
	Q	Diez, S., Ludwig, R., and Weber, H.G., "All-Optical Switch for TDM and WDM/TDM Systems Demonstrated in a 640 Gbit/s Demultiplexing Experiment," <i>Electronics Letters</i> , Vol. 34, No. 8, Pgs. 803-805, April 16, 1988.
	R	Diez, S., Ludwig, R., and Weber, H.G., "Gain-Transparent SOA-Switch for High-Bitrate OTDM Add/Drop Multiplexing," <i>IEEE Photonics Technology Letters</i> , Vol. 11, No. 1, Pgs. 60-62, January 1999.
	S	Diez, S., Ludwig, R., Patzak, E., and Weber, H.G., "Novel Gain-Transparent SOA-Switch for High Bitrate OTDM Add/Drop Multiplexing," <i>ECOC'98</i> , Vol. 1, Pages 461-462, September 1998.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.PTO-1449
REV: 02/01

21153/05927/DOCS/1263424.1

FORM PTO-1449
(REV. 6-89)DEPARTMENT OF COMMERCE
Patent and Trademark Office

Attorney's Docket No.

21153-05927

Serial No.

10/020,558

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Applicants

Sol P. DiJaili et al.

Filing Date

December 14, 2001

Group Art Unit

2811

OTHER DOCUMENTS (Continued) (Including Author, Title, Date, Pertinent Pages, Etc.)

T	Dorgeuille, F., Noirie, L., Faure, J-P., Ambrosy, A., Rabaron, S., Boubal, F., Schilling, M., and Artigue, C., "1.28 Tbit/s Throughput 8x8 Optical Switch Based on Arrays of Gain-Clamped Semiconductor Optical Amplifier Gates," Optical Fiber Communication Conference, Vol. 4, Pages 221-223, March 2000.
U	Dorgeuille, F., Lavigne, B., Emery, J.Y., Di Maggio, M., Le Bris, J., Chiaroni, D., Renaud, M., Baucknecht, R., Schneibel, H.P., Graf, C., and Melchior, H., "Fast Optical Amplifier Gate Array for WDM Routing and Switching Applications," OFC '98 Technical Digest, Pages 42-44, 1998.
V	Doussiere, P., Jourdan, A., Soulage, G., Garabédian, P., Graver, C., Fillion, T., Derouin, E., and Leclerc, D., "Clamped Gain Travelling Wave Semiconductor Optical Amplifier for Wavelength Division Multiplexing Application," IEEE, US, Vol. Conf. 14, Pages 185-186, New York, September 14, 1994.
W	Evankow, Jr., J.D., and Thompson, R. A., "Photonic Switching Modules Designed with Laser Diode Amplifiers," IEEE, Journal on Selected Areas in Communications, Vol. 6, No. 7, Pages 1087-1095, August 1988.
X	Fernier, B., Brosson, P., Bayart, D., Doussière, P., Beaumont, R., Leblond, F., Morin, P., Da Loura, G., Jacquet, J., Derouin, E., and Garabedian, P., "Fast (300 ps) Polarization Insensitive Semiconductor Optical Amplifier Switch with Low Driving Current (70 mA)," Semiconductor Laser Conference, Conference Digest, 13 th IEEE International, Pages 130-131, September 21-25, 1992.
Y	Fouquet, J.E., Venkatesh, S., Troll, M., Chen, D., Schiaffino, S., and Barth, P.W., "Compact, Scalable Fiber Optic Cross-Connect Switches," IEEE, 1999 Digest of the LEOS Summer Topical Meetings, Pages 59-60, 1999.
Z	Ibrahim, M.M., "Photonic Switch Using Surface-Emitting Laser Diode and APD," 16 th National Radio Science Conference, NRSC'99, Pages 1-8, Ain Shams University, Cairo, Egypt, February 23-25, 1999.
A1	Jeong, G., and Goodman, J.W., "Gain Optimization in Switches Based on Semiconductor Optical Amplifiers," Journal of Lightwave Technology, Vol. 13, No. 4, Pages 598-605, April 1995.
B1	Kitamura, S., Hatakeyama, H., and Hamamoto, K., "Spot-Size Converter Integrated Semiconductor Optical Amplifiers for Optical Gate Applications," IEEE Journal of Quantum Electronics, Vol. 35, No. 7, Pages 1067-1074, July 1999.
C1	Leuthold, J., Besse, P.A., Eckner, J., Gamper, E., Dülk, M., and Melchior, H., "All-Optical Space Switches with Gain and Principally Ideal Extinction Ratios," IEEE Journal of Quantum Electronics, Vol. 34, No. 4, Pages 622-633, April 1998.
D1	McAdams, L.R., Weverka, R.T., and Cloonan, J., "Linearizing High Performance Semiconductor Optical Amplifiers: Techniques and Performance," LEOS Presentation, Pages 363-364, 1996.
E1	Mørk, J., and Mecozzi, A., "Semiconductor Devices for All-Optical Signal Processing: Just How Fast Can They Go?," IEEE Lasers and Electro-Optics Society 1999 12 th Annual Meeting, LEOS'99, Vol. 2, Pages 900-901, November 8-11, 1999.
F1	Mutalik, V. G., van den Hoven, G., and Tiemeijer, L., "Analog Performance of 1310-nm Gain-Clamped Semiconductor Optical Amplifiers," OFC '97 Technical Digest, Pages 266-267, 1997.
G1	Panajotov, K., Ryvkin, B., Peeters, M., Verschaffelt, G., Danckaert, J., Thienpont, H., Veretennicoff, I., "Polarisation Switching in Proton-Implanted VCSELs," 1999 Digest of the LEOS Summer Topical Meetings, Pages 55-56, July 26-30, 1999.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered.
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FORM PTO-1449 (REV. 6-89) INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)	U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office		Attorney's Docket No. 21153-05927	Serial No. 10/020,558
	Applicants Sol P. DiJaili et al.			
	Filing Date December 14, 2001		Group Art Unit 2811	

OTHER DOCUMENTS (Continued) (Including Author, Title, Date, Pertinent Pages, Etc.)		
H1	Qui, B.C., Ke, M.L., Kowalski, O.P., Bryce, A.C., Aitchison, J.S., Marsh, J.H., Owen, M., White, I.H., and Penty, R.V., "Monolithically Integrated Fabrication of 2x2 and 4x4 Crosspoint Switches Using Quantum Well Intermixing," 2000 International Conference on Indium Phosphide and Related Materials, Conference Proceedings, Pages 415-418, May 14-18, 2000.	
I1	Scheuer, J., Arbel, D., and Orenstein, M., "Nonlinear On-Switching of High Spatial Frequency Patterns in Ring Vertical Cavity Surface Emitting Lasers," 1999 IEEE LEOS Annual Meeting Conference Proceedings, 12 th Annual Meeting, IEEE Lasers and Electro-Optics Society 1999 Annual Meeting, Vol. 1, Pages 123-124, November 8-9, 1999.	
J1	Soto, H., Erasme, D., and Guekos, G., "All-Optical Switch Demonstration Using a Birefringence Effect in a Semiconductor Optical Amplifier," IEEE CLEO, Pacific Rim '99, Pages 888-889, 1999.	
K1	Soulage, G., Doussi�re, P., Jourdan, A., and Sotom, M., "Clamped Gain Travelling Wave Semiconductor Optical Amplifier as a Large Dynamic Range Optical Gate," Alcatel Alsthom Recherche, route de Nozay, 91460 Marcoussis (France), 4 unnumbered pages, undated.	
L1	Tai, C., and Way, W.I., "Dynamic Range and Switching Speed Limitations of an N x N Optical Packet Switch Based on Low-Gain Semiconductor Optical Amplifiers," IEEE Journal of Lightwave Technology, Vol. 14, No. 4, Pages 525-533, April 4, 1996.	
M1	Tiemeijer, L.F., Walczyk, S., Verboven, A.J.M., van den Hoven, G.N., Thijs, P.J.A., van Dongen, T., Binsma, J.J.M., and Jansen, E.J., "High-Gain 1310 nm Semiconductor Optical Amplifier Modules with a Built-in Amplified Signal Monitor for Optical Gain Control," IEEE Photonics Technology Letters, Vol. 9, No. 3, Pages 309-311, March 1997.	
N1	Toptchiyski, G., Kindt, S., and Petermann, K., "Time-Domain Modeling of Semiconductor Optical Amplifiers for OTDM Applications," IEEE Journal of Lightwave Technology, Vol. 17, No. 12, Pages 2577-2583, December 1999.	
O1	Tiemeijer, L.F., Thijs, P.J.A., Dongen, T.v., Binsma, J.J.M., Jansen, E.J., van Helleputte, H.R.J.R., "Reduced Intermodulation Distortion in 1300 nm Gain-Clamped MQW Laser Amplifiers," IEEE Photonics Technology Letters, Vol. 7, No. 3, Pages 284-286, March 1995.	
P1	van Roijen, R., van der Heijden, M.M., Tiemeijer, L.F., Thijs, P.J.A., van Dongen, T., Binsma, J.J.M., and Verbeek, B.H., "Over 15 dB Gain from a Monolithically Integrated Optical Switch with an Amplifier," IEEE Photonics Technology Letters, Vol. 5, No. 5, Pages 529-531, May 1993.	
Q1	Yoshimoto, N., Magari, K., Ito, T., Kawaguchi, Y., Kishi, K., Kondo, Y., Kadota, Y., Mitomi, O., Yoshikuni, Y., Hasumi, Y., Tohmori, Y., and Nakajima O., "Spot-Size Converted Polarization-Insensitive SOA Gate with a Vertical Tapered Submicrometer Stripe Structure," IEEE Photonics Technology Letters, Vol. 10, No. 4, Pages 510-512, April 4, 1998.	

EXAMINER	DATE CONSIDERED
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